IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously presented) A method, comprising:

   (a) measuring a skew between a data signal and a clock signal at a receiving side of a serial link implemented with a first semiconductor chip;

   (b) programming a phase relationship into a second semiconductor chip; and,

   (c) adjusting a phase relationship between said data signal and said clock signal to reduce said skew, wherein said adjusting of said phase relationship occurs at a transmitting side of said serial link implemented with said second semiconductor chip.

2. (Cancelled)

3. (Previously presented) The method of claim 1 further comprising receiving said measured skew at a skew adjustment unit implemented with said second semiconductor chip, and determining said phase relationship before said adjusting a phase relationship.

4. (Cancelled)

5. (Original) The method of claim 1 wherein said adjusting a phase relationship further comprises imposing a delay on at least one of said signals.

6. (Original) The method of claim 5 wherein said adjusting a phase relationship further comprises imposing a delay on both of said signals.

7. (Original) The method of claim 1 wherein said adjusting a phase relationship further comprises adjusting a phase offset between a pair of phasors associated with a pair of phase interpolators, a first of said phasors used to derive a second clock signal that times the transmission of said data signal, a second of said phasors used to derive said clock signal.

8. (Currently amended) An apparatus, comprising:

(a) a transmitter coupled to a receiver by a serial link, said serial link comprising a clock signal line and a data signal line to transport a clock signal and a data signal;

(b) a programmable delay unit within said transmitter, said programmable delay unit coupled to said skew adjustment circuitry, said programmable delay unit having an output node to provide one of said signals[[.]];

(c) skew measurement circuitry coupled to said serial link, said skew measurement circuitry coupled to said serial link closer to said receiver than said transmitter, said skew measurement circuitry to measure a skew

between said clock signal and said data signal, said skew measurement circuitry implemented with a first semiconductor chip; and

(d) skew adjustment circuitry coupled to said skew measurement circuitry and said transmitter, said skew adjustment circuitry to adjust said skew at a transmitting side of said serial link in response to a signal from said skew measurement circuitry, said transmitter and said skew adjustment circuitry implemented with a second semiconductor chip.

9. (Cancelled)

10. (Currently amended) The apparatus of claim 8 further comprising a second programmable delay unit within said transmitter, said second programmable delay unit coupled to said skew adjustment circuitry, said second programmable delay unit having an output node to provide another of said signals.

11. (Original) The apparatus of claim 9 wherein said programmable delay unit further comprises a cascade of inverters.

12. (Original) The apparatus of claim 11 wherein each of said inverters within said cascade of inverters has an adjustable propagation delay.

13. (Previously presented) The apparatus of claim 8 wherein transmission of said data signal is timed according to a phase interpolator output signal.

14. (Previously presented) The apparatus of claim 8 wherein said clock signal is derived from a phase interpolator output signal.

15. (Previously presented) The apparatus of claim 14 wherein said phase interpolator further comprises a skew control input that adjusts a phasor phase offset, said skew control input coupled to said skew adjustment circuitry.

16. (Previously presented) The apparatus of claim 8 wherein said skew adjustment circuitry further comprises a CPU.

17. (Previously presented) An apparatus, comprising:

(a) a network interface coupled to a transmitter;

(b) a receiver coupled to said transmitter by a serial link, said serial link comprising a clock signal line and a data signal line to transport a clock signal and a data signal, said receiver implemented with a first semiconductor chip;

(c) skew measurement circuitry coupled to said serial link, said skew measurement circuitry implemented with said first semiconductor chip and,

(d) skew adjustment circuitry coupled to said skew measurement circuitry and said transmitter, said skew adjustment circuitry to adjust said skew at a transmitting side of said serial link in response to a signal from said skew

measurement circuitry, said skew adjustment circuitry including a programmable phase relationship, said skew adjustment circuitry and said transmitter implemented with said second semiconductor chip.

18. (Original) The apparatus of claim 17 wherein transmission of said data signal is timed according to a phase interpolator output.

19. (Previously presented) The apparatus of claim 17 wherein said clock signal is derived from a phase interpolator output.

20. (Previously presented) The apparatus of claim 19 wherein said phase interpolator further comprises a skew control input to adjust a phasor phase offset, said skew control input coupled to said skew adjustment circuitry.

21. (Previously presented) The apparatus of claim 17 wherein said skew adjustment circuitry further comprises a CPU.

22. (Previously presented) The apparatus of claim 17 wherein said transmitter further comprises a parallel to serial converter to craft said data signal, said parallel to serial converter coupled to said network interface to receive parallel data.

23. (Original) The apparatus of claim 17 wherein said network interface corresponds to a physical layer.

24. (Original) The apparatus of claim 17 wherein said network interface corresponds to a media access control layer.

25. (Previously presented) A semiconductor chip comprising:

a) a serial link transmitter comprising a serial clock signal output and a serial data signal output, said serial link transmitter comprises a programmable delay unit having an output node from which said serial link clock signal flows;

b) skew adjustment circuitry coupled to said serial link transmitter, said skew adjustment circuitry to adjust a skew between said serial clock signal and said serial data signal, said skew adjustment circuitry comprising an input node to receive an indication of said skew from another semiconductor chip.

26. (Cancelled)

27. (Previously presented) The semiconductor chip of claim 26 wherein said programmable delay unit comprises a cascade of inverters.

28. (Previously presented) The semiconductor chip of claim 25 wherein said transmitter comprises a phase interpolator to time the transmission of said data signal.

29. (Previously presented) The semiconductor chip of claim 25 wherein said transmitter comprises a phase interpolator to time the transmission of said clock signal.